CLAIMS

What is claimed is:

1. The first stage of a preamplifier circuit, comprising :

a first differential pair of transistors and a second differential pair of transistors;

the bases of the first differential pair of amplifying transistors being capacitively coupled to the first side of an input through a first capacitor;

the bases of the second differential pair of amplifying transistors being capacitively coupled to the second side of an input through a second capacitor;

a first current loop and a second current loop;

the first current loop comprised of a first resistor, a first transistor switch and a second resistor;

the first resistor and second resistor having the same value;

the second current loop comprised of a third resistor, a second transistor switch and a fourth resistor;

the third resistor and fourth resistor having the same value;

the first current loop being coupled to the bases of a first differential pair of amplifying transistors;

the second current loop being coupled to the bases of a second differential pair of amplifying transistors;

a third transistor switch being coupled across the bases of the first differential pair of amplifying transistors;

a fourth transistor switch being coupled across the bases of the second differential pair of amplifying transistors; and

the first current loop and second current loop operable to equalize the charges upon the first transistor and second transistor.

2. The first stage of a preamplifier circuit of Claim 1, further comprising:

a base current compensation circuit responsively coupled to the bases of the first differential pair of amplifying transistors and the bases of the second differential pair of amplifying transistors.

3. The first stage of a preamplifier circuit of Claim 1, further comprising:

an MR sensor;

the first side of the MR sensor being coupled to the first terminal of the first capacitor; and

the second side of the MR sensor being coupled to the first terminal of the second capacitor.

4. The first stage of a preamplifier circuit of Claim 3, wherein the first current loop and second current loop operate to reduce the offset in differential current between each side of the amplifying circuits coupled to the MR sensor.

5. The first stage of a preamplifier circuit of Claim 3, further comprising use in a hard disk drive read/write amplifier circuit.

6. The first stage of a preamplifier circuit of Claim 1, wherein the first, second, third and fourth transistor switches are controlled by internal control circuits.

7. The first stage of a preamplifier circuit of Claim 1, wherein the first, second, third and fourth transistor switches further comprise MOS switches.

8. The first stage of a preamplifier circuit of Claim 7, wherein the first, second, third and fourth transistor switches further comprise either n-type transistors, p-type transistors or both.

9. An input preamplifier circuit stage, comprising:

a first circuit comprised of at least a first pair of differential transistors having an input and providing an output from the first stage of the preamplifier;

the first pair of differential transistors comprising a first amplifying transistor and a second amplifying transistor;

a second circuit comprised of at least a second pair of differential transistors having an input, being coupled to the first circuit, and providing an output from the first stage of the preamplifier;

the second pair of differential transistors comprising a third amplifying transistor and a fourth amplifying transistor;

the first circuit being coupled to the second circuit through the coupling of the collector of third amplifying transistor to the collector of the first amplifying transistor and the coupling of the collector of fourth amplifying transistor to the collector of the second amplifying transistor;

a first current loop within the first circuit;

a second current loop within the second circuit;

the first current loop comprising a first resistor with a first terminal and second terminal, a first transistor switch with an input and output and a second resistor with a first terminal and second terminal;

the first resistor and second resistor comprising a pair of balanced resistors;

the second terminal of the first resistor being coupled to the input of the first transistor switch;

the second terminal of the second resistor being coupled to the output of the first transistor switch;

the first terminal of the first resistor and the first terminal of the second resistor being coupled across the bases of the first pair of differential transistors;

a second transistor switch being coupled across the bases of the first amplifying transistor and the second amplifying transistor;

the second current loop within the second circuit comprising a third resistor with a first terminal and second terminal;

a third transistor switch with an input and output;

a fourth resistor with a first terminal and second terminal, the third and fourth resistors also comprising a pair of balanced resistors;

the second terminal of the third resistor being coupled to the input of the third transistor switch;

the second terminal of the fourth resistor being coupled to the output of the third transistor switch;

the first terminal of the third resistor and the first terminal of the fourth resistor being coupled across the bases of the second differential pair of transistors; and

a fourth transistor switch being coupled across the bases of the third amplifying transistor and the fourth amplifying transistor.

10. The input preamplifier circuit stage of Claim 9, further comprising

a base current compensation circuit responsively coupled to the bases of the first differential pair of amplifying transistors and the bases of the second differential pair of amplifying transistors; and

the base current compensation circuit being operable to equalize the current to the bases of the first differential pair of amplifying transistors and the bases of the second differential pair of amplifying transistors.

11. The input preamplifier circuit stage of Claim 10, further comprising:

an MR sensor; and

a means of capacitively coupling the MR sensor to the input of the first circuit and the input of the second circuit.

12. The input preamplifier circuit stage of Claim 11, further comprising:

the means of capacitively coupling the MR sensor to the input of the first circuit being a first capacitor;

the means of capacitively coupling the MR sensor to the input of the second circuit being a second capacitor;

the first side of the MR sensor being coupled to the first terminal of the first capacitor; and

the second side of the MR sensor being coupled to the first terminal of the second capacitor.

13. The input preamplifier circuit stage of Claim 12, wherein the first current loop and second current loop operate to reduce the offset in differential current between each side of the amplifying circuits coupled to the MR sensor.

14. The input preamplifier circuit stage of Claim 13, further comprising use in a hard disk drive read/write amplifier circuit.

15. The input preamplifier circuit stage of Claim 9, wherein the first, second, third and fourth transistor switches are controlled by internal control circuits.

16. The input preamplifier circuit stage of Claim 15, wherein the first, second, third and fourth transistor switches further comprise MOS transistors, bipolar transistors or either type of transistors.

17. The input preamplifier circuit stage of Claim 16, wherein the first, second, third and fourth transistor switches further comprise either n-type transistors, p-type transistors or both.

18. A method of reducing the offset current from a base current compensation circuit, comprising:

placing a current loop comprised of a balanced pair of resistors opposite each other and a pair of transistor switches opposite each other across the bases of a differential pair of transistors; and

capacitively coupling said current loop to the input of a circuit so that the current loop charges input capacitors so as to decrease the recovery time of the circuit.

19. The method for reducing the offset current from a base current compensation circuit of Claim 18, wherein said method is used in a MR preamplifier circuit.

20. The circuit for reducing the offset current from a base current compensation circuit of Claim 19, wherein said method is used in a hard disk drive circuit.